Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the claims:

Claim 1 (cancelled).

Claim 2 (currently amended). The PLL of claim ~~1~~ 5, further comprising a no signal present indicator coupled to the sync detector and to the loop filter, wherein the loop filter is further coupled to the vertical sync DTO.

Claim 3 (currently amended). The PLL of claim ~~1~~ 5, wherein the output logic is adapted to output the vertical sync.

Claim 4 (currently amended). The PLL of claim ~~1~~ 5, wherein the output logic is adapted to output a field identification.

Claim 5 (currently amended). ~~The PLL of claim 1~~ A vertical sync phase lock loop (PLL), comprising:

a sync detector;

a loop filter;

a vertical sync discrete time oscillator (DTO);

an output logic adapted to detect a vertical sync; the loop filter, the vertical sync DTO and the output logic being coupled to the sync detector; and

~~further comprising~~ a vertical sync equilibrium accumulator adapted to filter horizontal syncs and pass vertical syncs.

Claim 6 (currently amended). The PLL of claim 5, further comprising a sample block adapted to receive the vertical syncs, an end line input sample, and a mid line input sample, and is further adapted to output a sample at an end line and at a mid line, wherein the sample block is coupled to the vertical sync equilibrium accumulator and to the sync detector.

Claim 7 (original). The PLL of claim 6, wherein the sync detector is adapted to output a phase error, based on the received sample at the end line and at the mid line, to the loop filter.

Claim 8 (original). The PLL of claim 6, wherein the sync detector is adapted to output at least one of a following value from a group consisting of:

if a sync is detected, a lower than maximum value; and

if a sync is not detected, a maximum value;

based on the received sample at the end line and at the mid line, to the no signal present indicator.

Claim 9 (original). The PLL of claim 7, wherein the loop filter is adapted to output a vertical sync discrete time oscillator decrement value.

Claim 10 (currently amended). The PLL of claim 9, further comprising a vertical sync discrete time oscillator coupled to the loop filter and to the

sync detector, wherein the vertical sync discrete time oscillator is adapted to receive the vertical sync discrete time oscillator decrement value.

Claim 11 (original). The PLL of claim 10, wherein the vertical sync discrete time oscillator is adapted to produce a vertical sync discrete time oscillator value.

Claim 12 (original). The PLL of claim 11, wherein the phase error is further based on the vertical sync discrete time oscillator value.

Claim 13 (original). The PLL of claim 11, wherein the output vertical sync from the output logic is based on a received sync event from the sync detector and from the vertical sync discrete time oscillator value.

Claim 14 (currently amended). The PLL of claim ~~1~~ 5, wherein the PLL may be implemented in at least one of a following form from a group consisting of:

software;

hardware; and

a combination of software and hardware.

Claim 15 (cancelled).

Claim 16 (original). ~~The method of claim 15~~ A method for outputting a vertical sync, comprising:

receiving a vertical sync sample;

producing a total error based on the sample and a vertical sync discrete time oscillator (DTO) value;

driving a phase error, based on the vertical sync DTO value, to a minimum value; and

~~further comprising~~ producing a trigger level based on an average of a blank level and a sync level.

Claim 17 (currently amended). The method of claim 16, further comprising producing a trigger event at a falling edge zero crossing based on the trigger level and the sample.

Claim 18 (currently amended). The method of claim 17, further comprising producing a gradient error based on a difference between a sync height and the sample, wherein the sync height is based on the sync level, and wherein the gradient error allows effects of macrovision pseudosyncs to be ignored.

Claim 19 (currently amended). The method of claim 18, further comprising producing a position error based on the vertical sync DTO value.

Claim 20 (currently amended). The method of claim 19, further comprising storing the total error in a register, wherein the total error is based on an addition of the position error and the gradient error.

Claim 21 (currently amended). The method of claim 20, further comprising, if an underflow of the vertical sync DTO occurs, presetting the register to a maximum value.

Claim 22 (currently amended). The method of claim 21, further comprising issuing a potential sync event and updating the register if the total

error ~~138~~ corresponding with the trigger event is less than the total error stored previously in register.

Claim 23 (currently amended). The method of claim 22, further comprising storing the vertical sync DTO value at a second register during the potential sync event.

Claim 24 (currently amended). The method of claim 23, further comprising subtracting a half nominal DTO decrement value from the stored vertical sync DTO value to produce the phase error.

Claim 25 (currently amended). The method of claim 24, further comprising producing a proportional phase error term based on the phase error and a proportional gain constant.

Claim 26 (currently amended). The method of claim 25, further comprising producing a common mode integral phase error term based on the phase error and a common mode integral gain constant adapted to compensate for non standard number of lines per field.

Claim 27 (currently amended). The method of claim 26, further comprising producing a differential mode integral phase error term based on the phase error and a differential mode integral gain constant adapted to compensate for a different number of non standard half lines per field.

Claim 28 (currently amended). The method of claim 27, further comprising storing at a third register the vertical sync DTO value based on at least one of a following item from a group consisting of:

the proportional phase error term;

the common mode integral phase error term;

the differential mode integral phase error term; and

a nominal decrement value.

Claim 29 (currently amended). The method of claim 28, further comprising updating the third register at least at one of a following event from a group consisting of:

a point of underflow; and

a zero crossing.

Claim 30 (currently amended). The method of claim 29, further comprising causing a window that is centered on the zero crossing of the vertical sync DTO to open.

Claim 31 (currently amended). The method of claim 30, further comprising receiving the sync event by the window and checking for alignment of the sync event and the vertical sync output.

Claim 32 (currently amended). The method of claim 31, further comprising, if the sync event does not align with the vertical sync output, outputting the windowed sync event.

Claim 33 (currently amended). The method of claim 31, further comprising, if the sync event falls outside the window, outputting the vertical sync DTO zero crossing.

Claim 34 (currently amended). The method of claim 31, further comprising, if the sync event falls within the window, outputting the sync event.

Claim 35 (currently amended). The method of claim 31, further comprising outputting a field identifier.

Claim 36 (currently amended). The method of claim ~~15~~ 16, wherein the vertical sync sample is received at an end line and at a mid line.